REMARKS/ARGUMENT

Claim 4 has been amended to overcome the amendment identified by the Examiner.

Claim 2 has been amended better to define the claimed invention and overcome the 35 U.S.C. 112, second paragraph, rejection.

1) Claims 1-7, 9 and 11-16 stand rejected under 35 U.S.C. 102(b) as being anticipated by Baum et al. [4,928,239]. Applicants have amended independent Claims 1 and 11 to overcome the Baum reference.

In order that the rejection of Claims 1-7, 9 and 11-16 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." *Verdegall Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 1, as amended, requires and positively recites, a system, comprising: "a processor", "a memory coupled to the processor", "a stack that exists in the memory and contains stack data", "a memory controller coupled to the memory; wherein the processor issues data requests" and "wherein the memory controller adjusts memory management policies based on whether the data requests refer to stack data and

adjusting the memory management policies includes not allocating the cache line containing stack data within the cache memory, and forwarding the stack data from the secondary memory".

Independent Claim 11, as amended, requires and positively recites, a method of managing memory, comprising: "issuing a request for data", "indicating whether the requested data is stack data" and "varying the memory management policies depending on whether the requested data is stack data wherein **when the request for data is a read request for stack data reading data from a main memory without allocating a new cache line within the cache memory**, and forwarding the data to the processor".

The Examiner admits that Baum fails to teach that adjusting the memory management policies includes not allocating the cache line containing stack data within the cache memory (Office Action, page 7, lines 12-14). As such, Baum fails to teach "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference", as is required by law for a 35 USC 102(b) rejection. Accordingly, the 35 U.S.C. 102(b) rejection must be withdrawn since all of the elements of Claims 1 and 11 cannot be found in the Baum reference.

In his 35 U.S.C. 103(a) rejection of Claims 8 and 17, the Examiner relied upon Damron et al. as providing the above teaching not found in Baum. Applicants respectfully traverse any 35 U.S.C. 103(a) rejection of Claims 1 and 11, as amended, over Baum in view of Damron, as set forth below.

In proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing *In re Piasecki*, 745 F.2d 1468,

1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden **only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references**", *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing *In re Lalu*, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

Similarly, "obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, **absent some teaching or suggestion supporting the combination. Under section 103, teachings of references can be combined ONLY if there is some suggestion or incentive to do so.**" *ACS Hosp. Systems, Inc. v. Montefiore Hosp.*, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984).

Similarly, although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. **The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.** *In re Gordon*, 733 F.2d at 902, 221 USPQ at 1127. Moreover, **it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious.** *In re Gorman*, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985).

Baum teaches a cache memory with variable fetch and replacement schemes in which an instruction is presented to the cache; the instruction includes a cache control specifier which identifies a type of data being requested; based on the cache control

specifier, one of a plurality of replacement schemes is selected for swapping a data block out of the cache (Abstract, lines 1-5). Even if, arguendo, Baum discloses that the memory controller adjusts memory management policies based on whether the data requests refer to stack data (see col. 5, line 5 – col. 6, lines 16), as suggested by the Examiner, the management policies refer to: 1) standard replacement scheme for NORMAL data, standard replacement scheme being LRU (Least Recently Used) (col. 5, lines 37-42); 2) A STACK cache control specifier is used for stacked data structures that grow from low numbered addresses in memory – an example being Last-in-First-Out (LIFO) stack structure (col. 5, lines 48-51); 3) A SEQUENTIAL cache control specifier is used for sequential data access patterns such as those involved in block move of in scanning text (col. 6, lines 17-19); and 4) A PREFETCH cache control specifier is used to indicate that, in a LOAD or STORE to a first block, the next block, that is the block immediately following the first block in main memory 13, is very likely to be accessed in the near future (col. 6, lines 34-38).

Nowhere, however, does Baum teach or suggest, when the requested data is STACK data, "... **enabling data to be written to a first level of the memory without allocating data from a second level of the memory**", as required by Claim 1 OR "wherein **when the request for data is a read request for stack data reading data from a main memory without allocating a new cache line within the cache memory**", as required by Claim 11.

Damron's invention, on the other hand, relates to a completely different issue (cache pollution) caused by large chunks of streaming data that is solved by an additional bit of "streaming data" in the TAG information field. Even if, arguendo, Damron et al were to disclose a similar cache memory system and method wherein cache line containing stack data (Col. 4, lines 40-45; Col 11, Lines 20-23) is not allocated (Col 9, lines 12-14) to a cache memory (Fig. #A, Victim Cache 155) due to the access pattern and access frequency of

stack data ((Col 4, lines 40-52), in order to improve cache miss rate and system operation speed (Col 9, lines 15-20), as suggested by the Examiner, Damron does not teach or suggest the previously identified deficiency of the Baum reference, namely, Baum's failure to, when the requested data is STACK data, "... **enable data to be written to a first level of the memory without allocating data from a second level of the memory**", as required by Claims 1, OR "wherein **when the request for data is a read request for stack data reading data from a main memory without allocating a new cache line within the cache memory**", as required by Claim 11. As a result, there would be no motivation by those of ordinary skill in the art at the time of the invention to combine Baum and Damron, and even if actually were, the combination would not obviate the claimed invention.

Claims 2-7 and 9 stand allowable as depending (directly or indirectly) from allowable Claim 1 and by including further limitations not taught or suggested by the reference of record. Claims 12-16 stand allowable as depending (directly or indirectly) from allowable Claim 11 and by including further limitations not taught or suggested by the reference of record.

Claim 2, as amended, further defines the system of claim 1, wherein the first level of memory is faster than the second level of memory. Claim 2 depends from Claim 1 and is therefore allowable for the same reasons set forth above for the allowance of Claim 1.

Claim 3 further defines the system of claim 2, wherein the first level of memory comprises a cache memory that implements a cache allocation policy, and wherein the cache allocation policy is adjusted based on the type of data access requested. Claim 3 depends from Claim 2 and is therefore allowable for the same reasons set forth above for the allowance of Claim 2.

Claim 4 further defines the system of claim 3, wherein the allocation policy is adjusted when the type of data access refers to stack data that corresponds to a predetermined word in a cache line and the cache line is not present in the cache memory. There is no teaching whatsoever in Baum for an "allocation policy is adjusted when the type data access refers to stack data that corresponds to a predetermined word in a cache line and the cache line is not present in the cache memory". For this reason alone Claim 4 is allowable over the Baum reference. Moreover, Claim 4 depends from Claim 3 and is therefore allowable for the same reasons set forth above for the allowance of Claim 3.

Claim 5 further defines the system of claim 4, wherein the type of data request involves writing to the stack. Claim 5 depends from Claim 4 and is therefore allowable for the same reasons set forth above for the allowance of Claim 4.

Claim 6 further defines the system of claim 5, wherein adjusting the memory management policies includes allocating the cache line containing stack data within the cache memory, and updating the stack data within the cache line without fetching data from the secondary memory. Claim 6 depends from Claim 5 and is therefore allowable for the same reasons set forth above for the allowance of Claim 5.

Claim 7 further defines the system of claim 4, wherein the type of data request involves reading from the stack. Claim 7 depends from Claim 4 and is therefore allowable for the same reasons set forth above for the allowance of Claim 4.

Claim 9 further defines the system of claim 4, wherein the predetermined word is the first word in the cache line. Claim 9 depends from Claim 4 and is therefore allowable for the same reasons set forth above for the allowance of Claim 4.

Claim 12 further defines the method of claim 11, further comprising determining if the requested data corresponds to a predetermined word in a cache line in a cache memory. There is no teaching in Baum that "the requested data corresponds to a predetermined word in a cache line in a cache memory". For this reason alone, Claim 12 is allowable over the Baum reference. Moreover, Claim 12 depends from Claim 11 and is therefore allowable for the same reasons set forth above for the allowance of Claim 11.

Claim 13 further defines the method of claim 12, further comprising determining whether the request for data is a write request or a read request. Claim 13 depends from Claim 12 and is therefore allowable for the same reasons set forth above for the allowance of Claim 12.

Claim 14 further defines the method of claim 13, wherein the request for data is a write request for stack data and the method further comprises writing data to the cache line without fetching data from a main memory. There is no teaching in Baum that when "the request for data is a write request for stack data and the method further comprises writing data to the cache line without fetching data from a main memory". For this reason alone, Claim 14 is allowable over the Baum reference. Moreover, Claim 14 depends from Claim 13 and is therefore allowable for the same reasons set forth above for the allowance of Claim 13.

Claim 15 further defines the method of claim 14, wherein the predetermined word is the first word in the cache line. Claim 15 depends from Claim 14 and is therefore allowable for the same reasons set forth above for the allowance of Claim 14.

Claim 16 further defines the method of claim 14, further comprising enabling a valid bit associated with the cache line. There is no teaching in Baum for "enabling a valid bit associated with the cache line". For this reason alone, Claim 16 is allowable

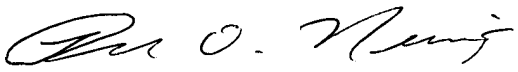
over Baum. Moreover, Claim 16 depends from Claim 14 and is therefore allowable for the same reasons set forth above for the allowance of Claim 14.

2) Claim 10 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Baum et al. Applicants respectfully traverse this rejection, as set forth below.

Claim 10 further defines the system of claim 4, wherein the predetermined word is the last word in the cache line. The base claim (claim 1) upon which Claim 10 depends has been amended to be allowable over Baum. Claim 10 is therefore allowable for the same reasons set forth above for the allowance of Claims 1 and 4.

Claims 1-7, 9-12 and 14-16 stand allowable in light of the amendments to Claims 1 and 11. New Claims 18 and 19 are similarly allowable over the cited art. Applicants respectfully request withdrawal of the rejections and allowance of the application at the earliest possible date.

Respectfully submitted,



Ronald O. Neerings
Reg. No. 34,227
Attorney for Applicants

TEXAS INSTRUMENTS INCORPORATED
P.O. BOX 655474, M/S 3999
Dallas, Texas 75265
Phone: 972/917-5299
Fax: 972/917-4418